

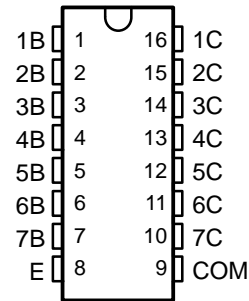
# ULN2001A THRU ULN2004A DARLINGTON TRANSISTOR ARRAYS

SLRS027 – D2624, DECEMBER 1976 – REVISED APRIL 1993

## HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- 500-mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay Driver Applications
- Designed to Be Interchangeable With Sprague ULN2001A Series

D OR N PACKAGE  
(TOP VIEW)

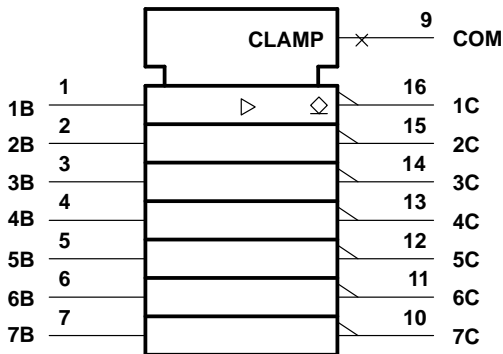


### description

The ULN2001A, ULN2002A, ULN2003A, and ULN2004A are monolithic high-voltage, high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. For 100-V (otherwise interchangeable) versions, see the SN75465 through SN75469.

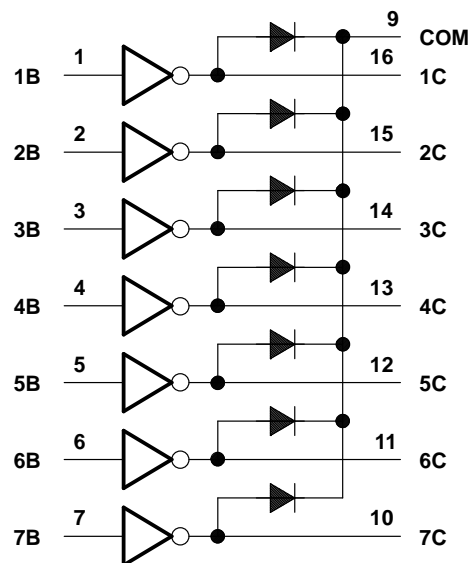
The ULN2001A is a general-purpose array and can be used with TTL, P-MOS, CMOS, and other MOS technologies. The ULN2002A is specifically designed for use with 14- to 25-V P-MOS devices. Each input of this device has a zener diode and resistor in series to control the input current to a safe limit. The ULN2003A has a 2.7-k $\Omega$  series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices. The ULN2004A has a 10.5-k $\Omega$  series base resistor to allow its operation directly from CMOS or P-MOS devices that use supply voltages of 6 to 15 V. The required input current of the ULN2004A is below that of the ULN2003A, and the required voltage is less than that required by the ULN2002A.

### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

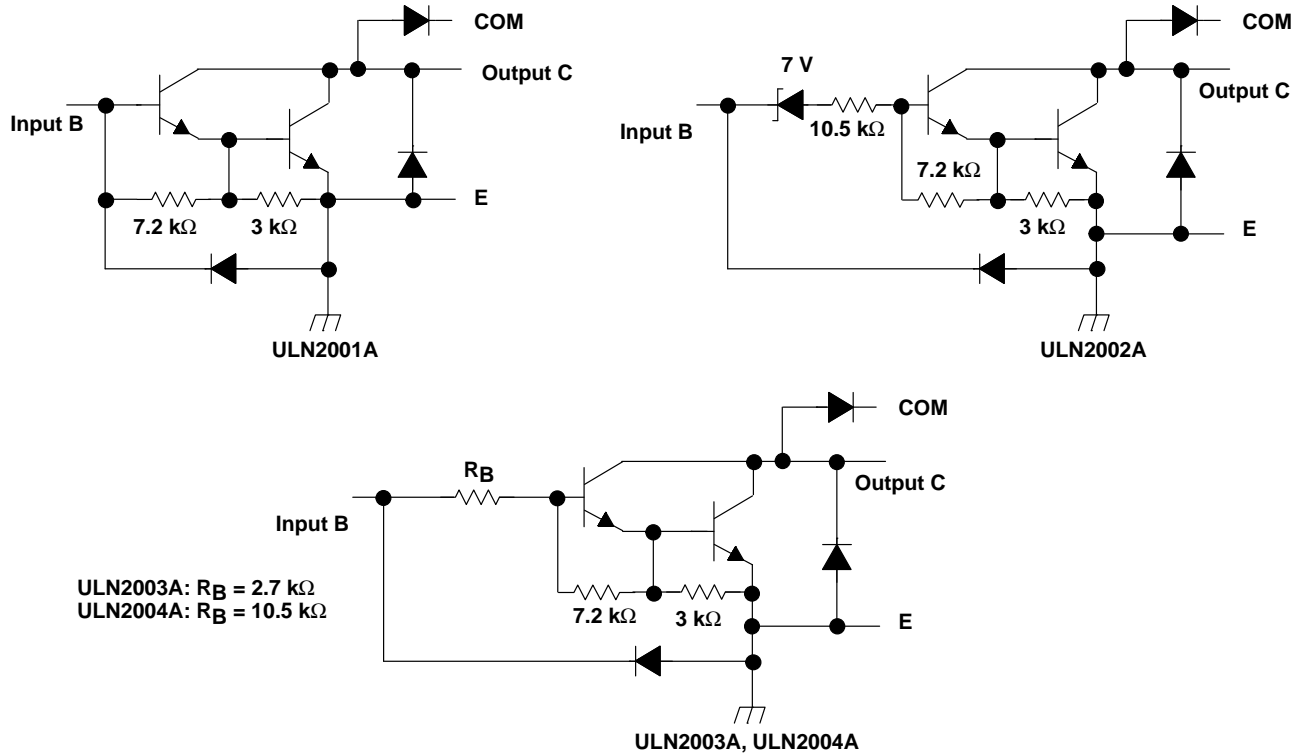
### logic diagram



# ULN2001A THRU ULN2004A DARLINGTON TRANSISTOR ARRAYS

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## schematics (each Darlington pair)



All resistor values shown are nominal.

## absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage .....	50 V
Input voltage, $V_I$ (see Note 1) .....	30 V
Peak collector current (see Figures 14 and 15) .....	500 mA
Output clamp current, $I_{OK}$ .....	500 mA
Total emitter-terminal current .....	-2.5 A
Continuous total power dissipation .....	See Dissipation Rating Table
Operating free-air temperature range .....	-20°C to 85°C
Storage temperature range .....	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .....	260°C

NOTE 1: All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	$T_A = 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW

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## electrical characteristics, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS	ULN2001A			ULN2002A			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
$V_{I(\text{on})}$ On-state input voltage	6	$V_{CE} = 2\text{ V}$ , $I_C = 300\text{ mA}$						13	V	
$V_{CE(\text{sat})}$ Collector-emitter saturation voltage	5	$I_I = 250\ \mu\text{A}$ , $I_C = 100\text{ mA}$	0.9	1.1		0.9	1.1		V	
		$I_I = 350\ \mu\text{A}$ , $I_C = 200\text{ mA}$	1	1.3		1	1.3			
		$I_I = 500\ \mu\text{A}$ , $I_C = 350\text{ mA}$	1.2	1.6		1.2	1.6			
$V_F$ Clamp forward voltage	8	$I_F = 350\text{ mA}$	1.7	2		1.7	2	V		
$I_{CEX}$ Collector cutoff current	1	$V_{CE} = 50\text{ V}$ , $I_I = 0$			50			50	$\mu\text{A}$	
	2	$V_{CE} = 50\text{ V}$ , $T_A = 70^\circ\text{C}$ , $V_I = 6\text{ V}$			100			100		
$I_{I(\text{off})}$ Off-state input current	3	$V_{CE} = 50\text{ V}$ , $T_A = 70^\circ\text{C}$ , $I_C = 500\ \mu\text{A}$	50	65		50	65		$\mu\text{A}$	
$I_I$ Input current	4	$V_I = 17\text{ V}$				0.82	1.25		mA	
$I_R$ Clamp reverse current	7	$V_R = 50\text{ V}$ , $T_A = 70^\circ\text{C}$			100			100	$\mu\text{A}$	
$h_{FE}$ Static forward current transfer ratio	5	$V_{CE} = 2\text{ V}$ , $I_C = 350\text{ mA}$	1000							
$I_R$ Clamp reverse current	7	$V_R = 50\text{ V}$			50			50	$\mu\text{A}$	
$C_i$ Input capacitance		$V_I = 0$ , $f = 1\text{ MHz}$			15	25		15	25	pF

## electrical characteristics, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS	ULN2003A			ULN2004A			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
$V_{I(\text{on})}$ On-state input voltage	6	$V_{CE} = 2\text{ V}$	$I_C = 125\text{ mA}$						5	V
			$I_C = 200\text{ mA}$			2.4			6	
			$I_C = 250\text{ mA}$			2.7			7	
			$I_C = 300\text{ mA}$			3				
			$I_C = 350\text{ mA}$						8	
$V_{CE(\text{sat})}$ Collector-emitter saturation voltage	5	$I_I = 250\ \mu\text{A}$ , $I_C = 100\text{ mA}$	0.9	1.1		0.9	1.1		V	
		$I_I = 350\ \mu\text{A}$ , $I_C = 200\text{ mA}$	1	1.3		1	1.3			
		$I_I = 500\ \mu\text{A}$ , $I_C = 350\text{ mA}$	1.2	1.6		1.2	1.6			
$I_{CEX}$ Collector cutoff current	1	$V_{CE} = 50\text{ V}$ , $I_I = 0$			50			50	$\mu\text{A}$	
	2	$V_{CE} = 50\text{ V}$ , $T_A = 70^\circ\text{C}$ , $V_I = 1\text{ V}$			100			100		
$V_F$ Clamp forward voltage	8	$I_F = 350\text{ mA}$	1.7	2		1.7	2	V		
$I_{I(\text{off})}$ Off-state input current	3	$V_{CE} = 50\text{ V}$ , $T_A = 70^\circ\text{C}$ , $I_C = 500\ \mu\text{A}$	50	65		50	65		$\mu\text{A}$	
$I_I$ Input current	4	$V_I = 3.85\text{ V}$	0.93	1.35					mA	
		$V_I = 5\text{ V}$				0.35	0.5			
		$V_I = 12\text{ V}$				1	1.45			
$I_R$ Clamp reverse current	7	$V_R = 50\text{ V}$			50			50	$\mu\text{A}$	
		$V_R = 50\text{ V}$ , $T_A = 70^\circ\text{C}$			100			100		
$C_i$ Input capacitance		$V_I = 0$ , $f = 1\text{ MHz}$			15	25		15	25	pF



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## switching characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output	See Figure 9		0.25	1	$\mu\text{s}$
$t_{PHL}$	Propagation delay time, high-to-low-level output			0.25	1	$\mu\text{s}$
$V_{OH}$	High-level output voltage after switching	$V_S = 50\text{ V}$ , $I_O \approx 300\text{ mA}$ , See Figure 10	$V_S - 20$			mV

## PARAMETER MEASUREMENT INFORMATION

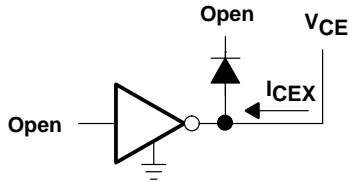


Figure 1.  $I_{CEX}$  Test Circuit

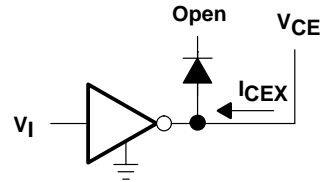


Figure 2.  $I_{CEX}$  Test Circuit

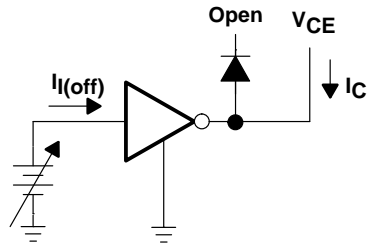


Figure 3.  $I_{I(off)}$  Test Circuit

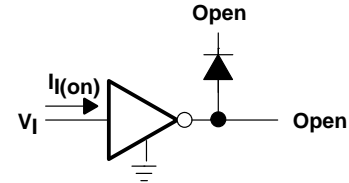
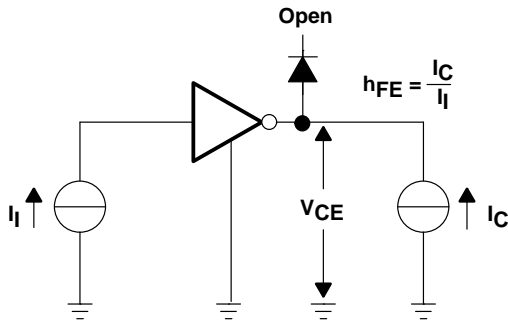


Figure 4.  $I_I$  Test Circuit



NOTE:  $I_I$  is fixed for measuring  $V_{CE(sat)}$ , variable for measuring  $h_{FE}$ .

Figure 5.  $h_{FE}$ ,  $V_{CE(sat)}$  Test Circuit

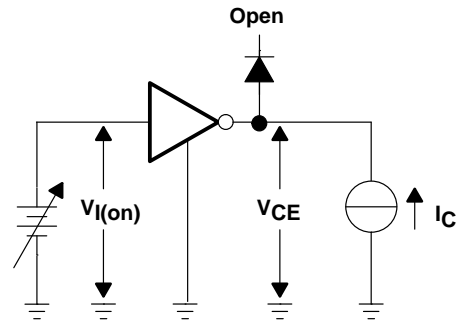


Figure 6.  $V_{I(on)}$  Test Circuit

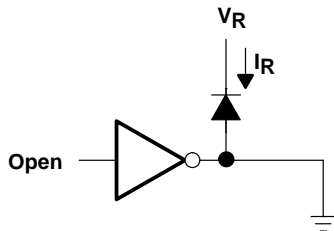


Figure 7.  $I_R$  Test Circuit

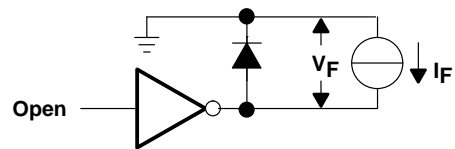


Figure 8.  $V_F$  Test Circuit

PARAMETER MEASUREMENT INFORMATION

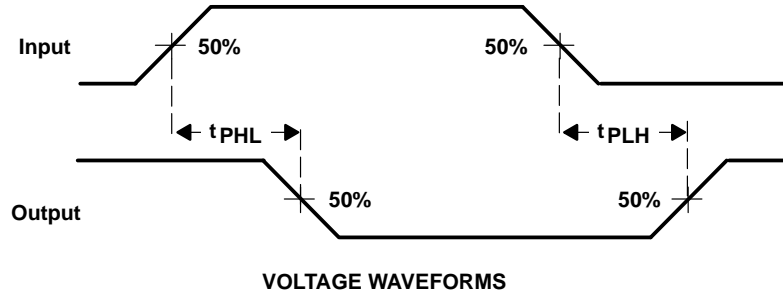
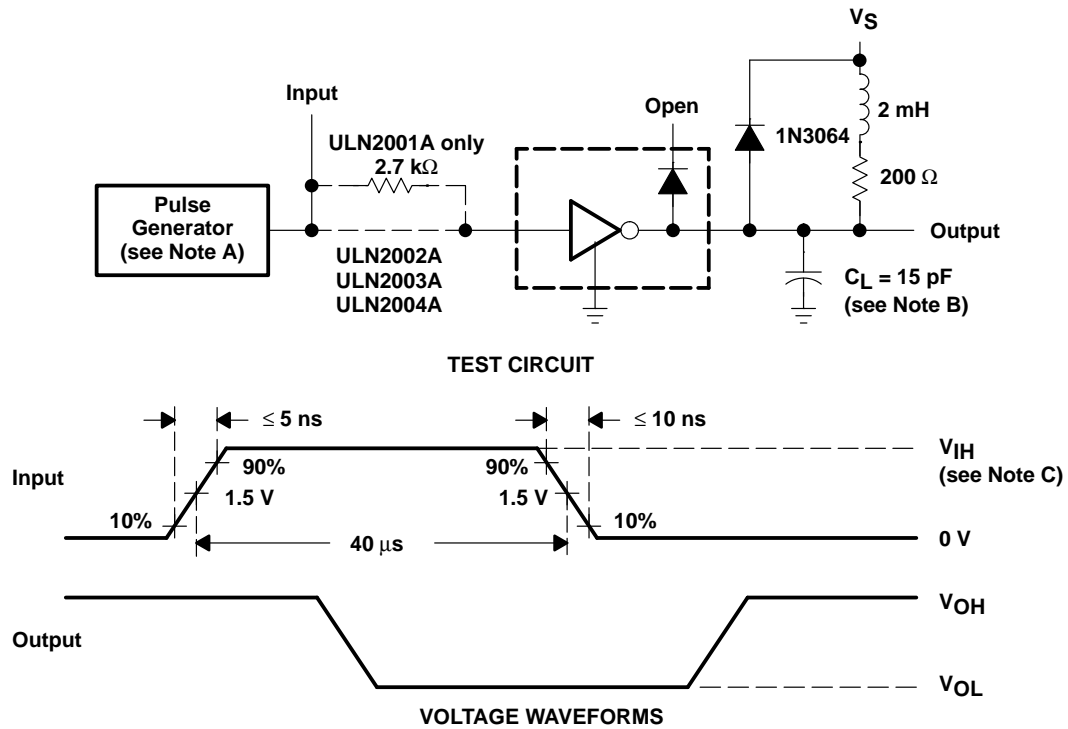


Figure 9. Propagation Delay Time Waveforms



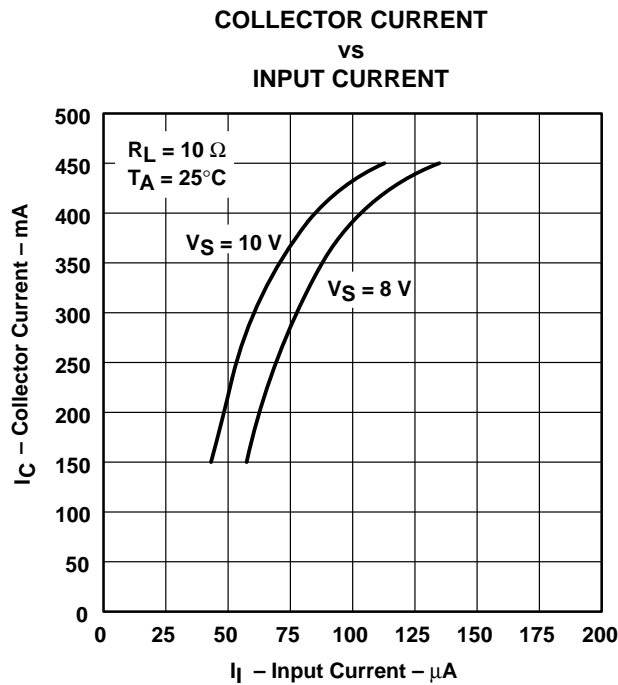
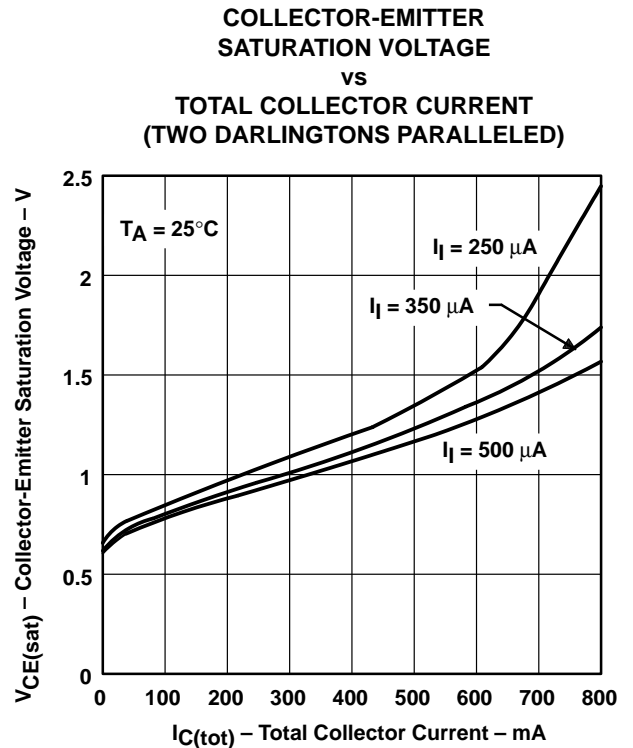
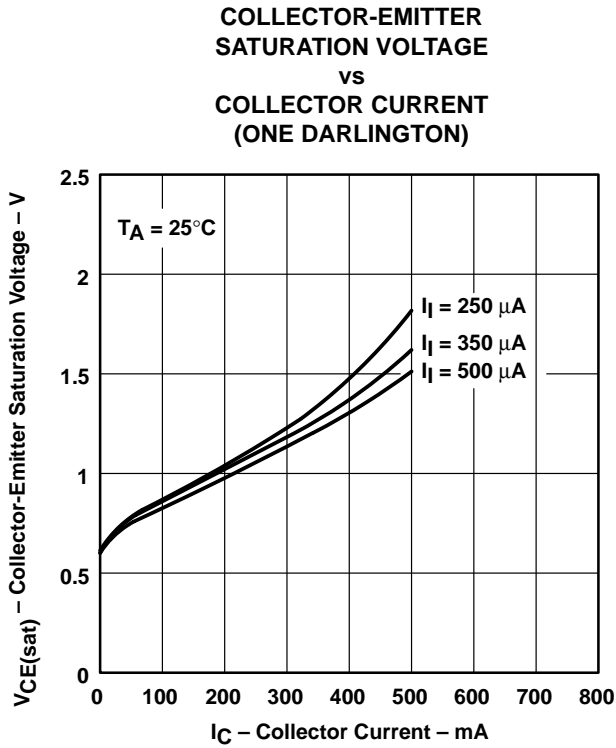
- NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz,  $Z_0 = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.  
 C. For testing the ULN2001A and the ULN2003A,  $V_{IH} = 3 \text{ V}$ ; for the ULN2002A,  $V_{IH} = 13 \text{ V}$ ; for the ULN2004A,  $V_{IH} = 8 \text{ V}$ .

Figure 10. Latch-Up Test Circuit and Voltage Waveforms

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## TYPICAL CHARACTERISTICS



THERMAL INFORMATION

D PACKAGE  
MAXIMUM COLLECTOR CURRENT  
VS  
DUTY CYCLE

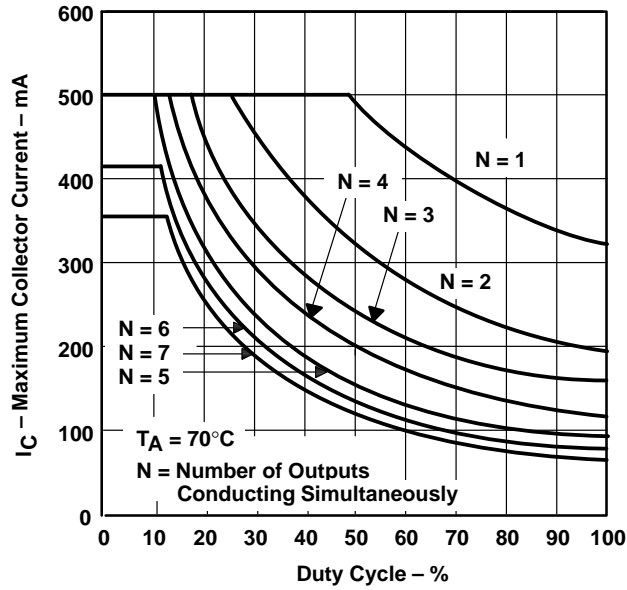


Figure 14

N PACKAGE  
MAXIMUM COLLECTOR CURRENT  
VS  
DUTY CYCLE

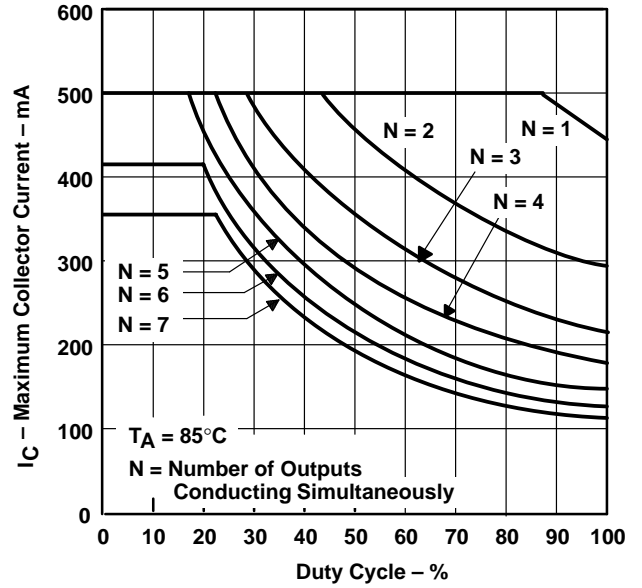


Figure 15

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## APPLICATION INFORMATION

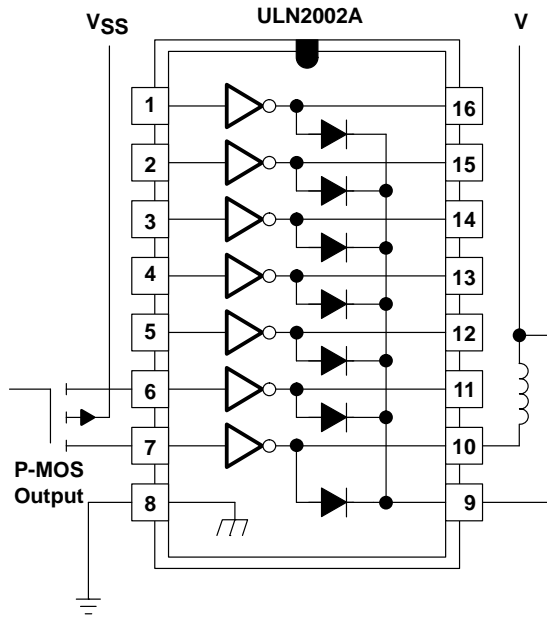


Figure 16. P-MOS to Load

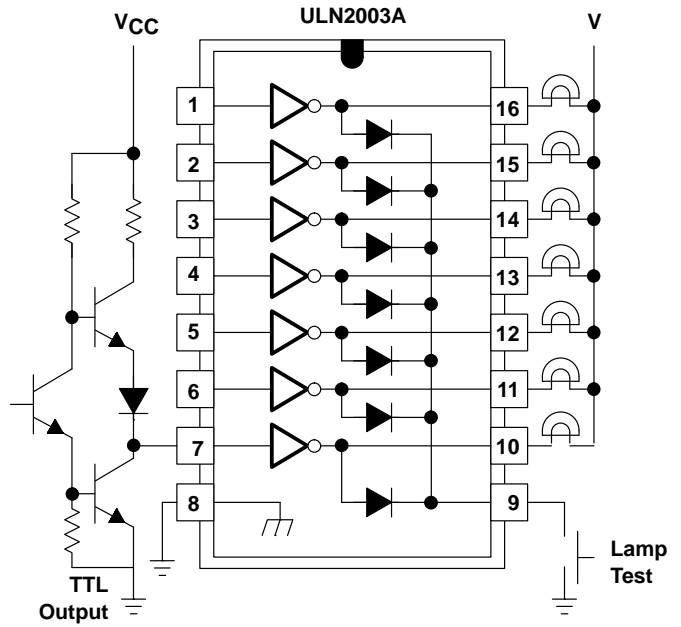


Figure 17. TTL to Load

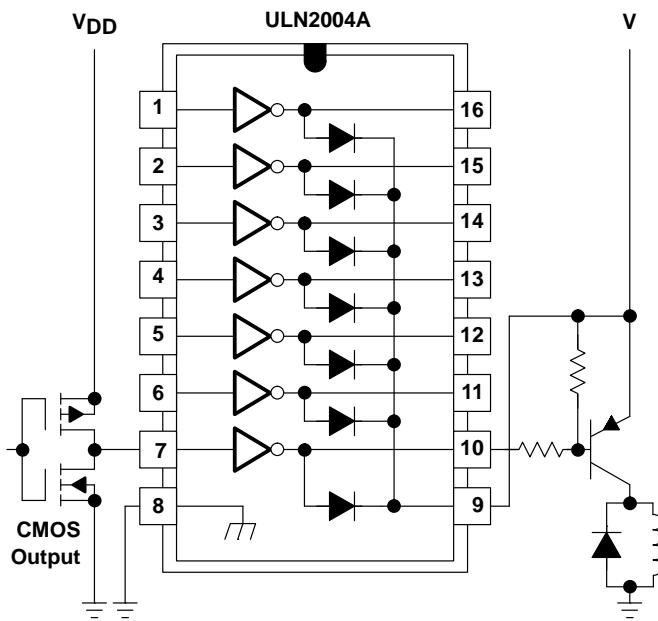


Figure 18. Buffer for Higher Current Loads

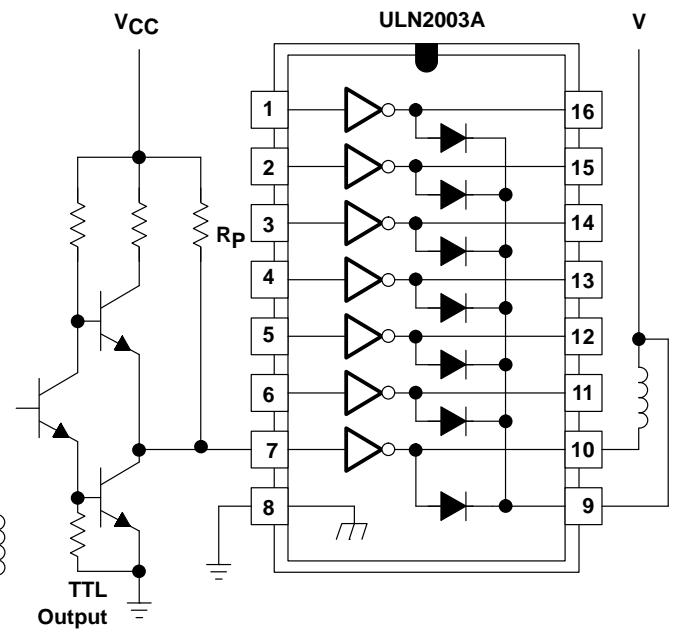


Figure 19. Use of Pullup Resistors to Increase Drive Current



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